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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
MEONSKE, TONIA L

ART UNIT	PAPER NUMBER
2183	

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DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,812	SHOEMAKER, KEN	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

2. Claims 10, 13, 16, and 19 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

3. Referring to claim 10, the limitation "executing said first inactive thread" doesn't tell us anything we don't already know from claim 9. In claim 9, line 4, the limitation "switching said first active thread with a first inactive thread" already tells us that the first inactive thread is being executed because when you switch to a thread this means that you begin executing the thread. Furthermore in claim 10, the limitation "executing ... said second active thread" doesn't claim anything we don't already know from claim 9. In claim 9, line 2, the limitation "fetching...a second active thread" indicates that the second active thread is already being executed.

4. Referring to claim 13, the limitation "executing the first inactive thread" doesn't tell us anything we don't already know from claim 9. In claim 9, line 4, the limitation "switching said first active thread with a first inactive thread" already tells us that the first inactive thread is being executed because when you switch to a thread this means that you begin executing the thread. Furthermore in claim 10, the limitation "executing ... said second inactive thread"

doesn't claim anything we don't already know from claim 9. In claim 12, line 2, the limitation "switching said second active thread with a second inactive thread" already tells us that the second inactive thread is being executed because when you switch to a thread this means that you begin executing the thread.

5. Referring to claim 16, the limitation "executing said first inactive thread" doesn't tell us anything we don't already know from claim 15. In claim 15, line 6, the limitation "switching said first active thread with a first inactive thread" already tells us that the first inactive thread is being executed because when you switch to a thread this means that you begin executing the thread. Furthermore the limitation "executing...said second active thread" doesn't claim anything we don't already know from claim 15. In claim 15, line 4, the limitation "fetching...a second active thread" indicates that the second active thread is already being executed.

6. Referring to claim 19, the limitation "executing the first inactive thread" doesn't tell us anything we don't already know from claim 9. In claim 15, line 6, the limitation "switching said first active thread with a first inactive thread" already tells us that the first inactive thread is being executed because when you switch to a thread this means that you begin executing the thread. Furthermore in claim 19, the limitation "executing ... said second inactive thread" doesn't claim anything we don't already know from claim 15. In claim 15, line 6, the limitation "switching said second active thread with a second inactive thread" already tells us that the second inactive thread is being executed because when you switch to a thread this means that you begin executing the thread. Appropriate correction is required.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 10, 13, 16, and 19 are objected to under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Referring to claim 10, the limitation "executing said first inactive thread" is unclear. In claim 9, switching to the inactive thread has already been claimed. When you switch to a thread the thread is now active and is executing. It is impossible to execute an inactive thread. Claims 13, 16, and 19 are also objected to for claiming the execution of an inactive thread. Appropriate correction is required.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-4 and 9-20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Simultaneous Multithreading: A Platform for Next-Generation Processors, Susan Eggers, et al. (hereinafter referred to as Eggers et al.).

12. Referring to claim 1, Eggers et al. have taught a multi-threading processor, comprising:

a. a first instruction fetch unit (Page 14, left hand column, The fetch unit partitions itself among the threads and has eight program counters.) and a second instruction fetch unit (Page 14, left hand column, The fetch unit partitions itself among the threads and has eight program counters.);

b. a multi-thread scheduler unit coupled to said first instruction fetch unit and said second instruction fetch unit (page 13, left hand column, see the description of Figure 1c);

c. an execution unit coupled to said scheduler unit, wherein said execution unit is to execute a first active thread and a second active thread (pages 13 and 14); and

d. a register file coupled to said execution unit (pages 14-15, see the section entitled "Register file and pipeline"), wherein said register file is to switch one of said first active thread and said second active thread with a first inactive thread (page 14, Eggars et al. have taught fetching from two threads each cycles. The fetch unit fetches what will provide the most benefit. The unit has eight threads and the disclosure has taught that any two of the eight thread can be selected during every cycle. Therefore this limitation is inherently taught.).

13. Referring to claim 2, Eggers et al. have taught a multi-threading processor as recited in claim 1, as described above, and further comprising an on deck context unit coupled to the register file, wherein said on deck context unit is to maintain a first inactive thread and a second inactive thread (page 15, hardware contexts for eight threads).

14. Referring to claim 3, Eggers et al. have taught a multi-threading processor as recited in claim 2, wherein said register file is to switch one of the first active thread and the second active thread with a second inactive thread (page 14, Eggers et al. have taught fetching from two threads each cycles. The fetch unit fetches what will provide the most benefit. The unit has eight threads and the disclosure has taught that any two of the eight thread can be selected during every cycle. Therefore this limitation is inherently taught.).

15. Referring to claim 4, Eggers et al. have taught a multi-threading processor as recited in claim 3, as described above, and further comprising:

a. a first instruction decode unit coupled between the first instruction fetch unit and the scheduler unit (page 14, first paragraph, the decoder for the first thread instructions); and

b. a second instruction decode unit coupled between the second instruction fetch unit and the scheduler unit (page 14, first paragraph, the decoder for the second thread instructions).

16. Referring to claim 9, Eggers et al. have taught a method for switching threads in a multi-threading processor, comprising:

a. fetching a first active thread and a active second thread (Page 14, left hand column);

b. detecting a stalling event in said first active thread (Page 14, left hand column, cache miss); and

c. switching said first active thread with a first inactive thread, if said first inactive thread is ready to execute (Page 14, left hand column, when a cache miss occurs, a thread switch occurs to provide the most immediate performance benefit.).

17. Referring to claim 10, Eggers et al. have taught a method for switching threads as recited in claim 9, as described above, and further comprising executing said first inactive thread and said second active thread (page 14, Eggars et al. have taught fetching from two threads each cycles. The fetch unit fetches what will provide the most benefit. The unit has eight threads and

the disclosure has taught that any two of the eight thread can be selected during every cycle. Therefore this limitation is inherently taught.).

18. Referring to claim 11, Eggers et al. have taught a method for switching threads as recited in claim 9, as described above, and further comprising detecting a stalling event in the second active thread (Page 14, left hand column, cache miss).

19. Referring to claim 12, Eggers et al. have taught a method for switching threads as recited in claim 11, as described above, and further comprising switching said second active thread with a second inactive thread, if said second inactive thread is ready to execute (page 14, Eggars et al. have taught fetching from two threads each cycles. The fetch unit fetches what will provide the most benefit. The unit has eight threads and the disclosure has taught that any two of the eight thread can be selected during every cycle. Therefore this limitation is inherently taught.).

20. Referring to claim 14, Eggers et al. have taught a method for switching threads as recited in claim 9, as described above, and further comprising executing the second active thread, if the first inactive thread is not ready to execute (page 14, Eggars et al. have taught fetching from two threads each cycles. The fetch unit fetches what will provide the most benefit. The unit has eight threads and the disclosure has taught that any two of the eight thread can be selected during every cycle. Therefore this limitation is inherently taught.).

21. Claim 13 does not recite limitations above the claimed invention set forth in claim 10 and is therefore rejected for the same reasons set forth in the rejection of claim 10 above.

22. Claim 15 does not recite limitations above the claimed invention set forth in claim 9 and is therefore rejected for the same reasons set forth in the rejection of claim 9 above.

23. Claim 16 does not recite limitations above the claimed invention set forth in claim 10 and is therefore rejected for the same reasons set forth in the rejection of claim 10 above.

24. Claim 17 does not recite limitations above the claimed invention set forth in claim 11 and is therefore rejected for the same reasons set forth in the rejection of claim 11 above.

25. Claim 18 does not recite limitations above the claimed invention set forth in claim 12 and is therefore rejected for the same reasons set forth in the rejection of claim 12 above.

26. Claim 19 does not recite limitations above the claimed invention set forth in claim 10 and is therefore rejected for the same reasons set forth in the rejection of claim 10 above.

27. Claim 20 does not recite limitations above the claimed invention set forth in claim 14 and is therefore rejected for the same reasons set forth in the rejection of claim 14 above.

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simultaneous Multithreading: A Platform for Next-Generation Processors, Susan Eggers, et al. (hereinafter referred to as Eggers et al.).

30. Referring to claim 5, Eggers et al. have taught a multi-threading processor as recited in claim 1, as described above. Eggers has not specifically taught wherein the scheduler unit is a four thread scheduler unit, further comprising: a third instruction fetch unit coupled to said four thread scheduler unit; and a fourth instruction fetch unit coupled to said four thread scheduler

unit. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Eggers et al. have any number of fetch units coupled to the scheduler, including a third and a fourth fetch unit, as it has been held that duplicating parts for multiple effect is not a patentable difference. *In re Harza,* 274 F .d 669, 671, 124 USPQ 378, 380 (CCPA 1960).

31. Referring to claim 6, Eggers et al. have taught a multi-threading processor as recited in claim 5, as described above. Eggers et al. have not specifically taught wherein said register file is a four way register file. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the register file of Eggers et al. be any number of ways, including four ways as it has been held that changing size is not a patentable difference. *In re Rose,* 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

32. Referring to claim 7, Eggers et al. have taught a multi-threading processor as recited in claim 6, as described above, and wherein said register file is to switch one of the first active thread and the second active thread with a second inactive thread (page 14, Eggars et al. have taught fetching from two threads each cycles. The fetch unit fetches what will provide the most benefit. The unit has eight threads and the disclosure has taught that any two of the eight thread can be selected during every cycle. Therefore this limitation is inherently taught.).

33. Referring to claim 8, Eggers et al. have taught a multi-threading processor as recited in claim 7, as described above. Eggers et al. have not specifically taught

a. a third instruction decode unit coupled between the third instruction fetch unit and the four thread scheduler unit; and

b. a fourth instruction decode unit coupled between the fourth instruction fetch unit and the four thread scheduler unit.

34. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Eggers et al. have any number of instruction decode units coupled the fetch units and the scheduler, including a third and a fourth instruction decode unit, as it has been held that duplicating parts for multiple effect is not a patentable difference. *In re Harza,* 274 F .d 669, 671, 124 USPQ 378, 380 (CCPA 1960).

Conclusion

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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